Notice of Allowability	Application No.	Applicant(s)	
	10/705,775	MAEDA ET AL.	
	Examiner	Art Unit	
	ROBERT R. RAINEY	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *papers received 8/10/2009*.

2. ☒ The allowed claim(s) is/are *1-3,6,11,14 and 19-22 now renumbered 1-10*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20090921*.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *New drawing sheet*.

/Amare Mengistu/
Supervisory Patent Examiner, Art Unit 2629

ALLOWANCE

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Deborah S. Gladstein on 9/17/09.

The application has been amended as follows:

In the claims:

Cancel claims 4, 5, 7-10, 12, 13, and 15-18

Replace claims 1-3, 6, 11, 14, 19, and 21 with the corresponding claims below.

1. A data signal line driving method where n, n>1, video signal lines supply a multiphased video signal in parallel to m, m>1, data fetching blocks, each data fetching block fetching the multiphased video signal into n data line groups and each data line group including p, p>1, sequential data signal lines and driving p corresponding sequentially adjoining sections of a display, the data signal lines each having an associated sampling switch that connects each data signal line to a video signal line such that the p sequential data signal lines of each data line group are connected to the same video signal line and p sequential data signal lines are alternately connected to the same video signal line with an interval of another ((n-1) x p) data signal lines therebetween, the p sampling switches associated with a given data line group each responsive to a different sampling pulse, and p shift registers provided with respect to each data fetching block

with the shift registers being connected between blocks such that the blocks are driven sequentially,

said method comprising:

fetching the multiphased video signal from the video signal lines, via p sampling pulses, into the data signal lines in each block in response to one or more timing pulses generated by the p shift registers provided with respect to the block, and driving the blocks sequentially, there being performed a first driving in which the p shift registers in each block are driven sequentially to provide p sequential timing pulses and each sampling pulse in the block being responsive to a corresponding timing pulse such that the sampling pulses in the block are activated sequentially, and there being performed a second driving in which only one shift register in the block is driven to provide one timing pulse and all sampling pulses in the block are responsive to the one timing pulse such that all sampling pulses in the block are activated simultaneously.

2. A data signal line driving method where n, n>1, video signal lines supply a multiphased video signal having a plurality of color signals in parallel to m, m>1, data fetching blocks, each data fetching block fetching the multiphased video signal into n data line groups and each data line group including p, p>1, sequential data signal lines and driving p corresponding sequentially adjoining sections of a display, the data signal lines each having an associated sampling switch that connects each data signal line to a video signal line such that the p sequential data signal lines of each data line group are connected to the same video signal line and p sequential data signal lines are alternately

connected to the same video signal line with an interval of another ((n-1) x p) data signal lines therebetween, the p sampling switches associated with a given data line group each responsive to a different sampling pulse, and p shift registers provided with respect to each data fetching block with the shift registers being connected between blocks such that the blocks are driven sequentially, each video signal line including a plurality of divisional video signal lines divided so as to respectively correspond to the color signals and each data signal line including a corresponding plurality of divisional data signal lines,

said method comprising:

fetching the multiphased video signal from the video signal lines, via p sampling pulses, into the data signal lines in each block in response to one or more timing pulses generated by the p shift registers provided with respect to the block, and driving the blocks sequentially, there being performed a first driving in which the p shift registers in each block are driven sequentially to provide p sequential timing pulses and each sampling pulse in the block being responsive to a corresponding timing pulse such that the sampling pulses in the block are activated sequentially, and there being performed a second driving in which only one shift register in the block is driven to provide one timing pulse and all sampling pulses in the block are responsive to the one timing pulse such that all sampling pulses in the block are activated simultaneously.

3. A data signal line driving circuit, which drives a plurality of data signal lines respectively so as to fetch a multiphased video signal supplied via n, n>1, video signal lines into the data signal lines, comprising:

m, m>1, data fetching blocks configured to receive a multiphased video signal supplied in parallel to the data fetching blocks by the video signal lines;

each data fetching block configured to fetch the multiphased video signal into n data line groups and each data line group including p, p>1, sequential data signal lines and driving p corresponding sequentially adjoining sections of a display;

a plurality of sampling switches, each sampling switch connecting a data signal line to a video signal line such that the p sequential data signal lines of each data line group are connected to the same video signal line and p sequential data signal lines are alternately connected to the same video signal line with an interval of another ((n-1) x p) data signal lines therebetween, the p sampling switches associated with a given data line group each configured to be responsive to a different sampling pulse;

p shift registers provided with respect to each data fetching block, the shift registers being connected between blocks such that the blocks are driven sequentially;

a sampling pulse generating section provided with respect to each data fetching block configured to generate p sampling pulses responsive to one or more timing pulses generated by the p shift registers provided with respect to the block, the p sampling pulses configured to fetch the multiphased video signal from the video signal lines into all data signal lines in the block;

the data signal line driving circuit performing:

a first driving in which the p shift registers in each block are driven sequentially to provide p sequential timing pulses and each sampling pulse in the block being responsive to a corresponding timing pulse such that the sampling pulses in the block are activated sequentially, and

a second driving in which only one shift register in the block is driven to provide one timing pulse and all sampling pulses in the block are responsive to the one timing pulse such that all sampling pulses in the block are activated simultaneously.

6. The data signal line driving circuit as set forth in claim 3, wherein the data signal line driving circuit includes stopping means for stopping operation of the shift registers not required in driving the data signal lines when performing the second driving.

11. A data signal line driving circuit, which drives a plurality of data signal lines respectively so as to fetch a multiphased video signal having a plurality of color signals supplied via n, n>1, video signal lines into the data signal lines, wherein each video signal line includes a plurality of divisional video signal lines divided so as to respectively correspond to the color signals and each data signal line includes a corresponding plurality of divisional data signal lines, comprising:

m, m>1, data fetching blocks configured to receive a multiphased video signal supplied in parallel to the data fetching blocks by the video signal lines;

each data fetching block configured to fetch the multiphased video signal into n data line groups and each data line group including p, p>1, sequential data signal lines and driving p corresponding sequentially adjoining sections of a display;

a plurality of sampling switches, each sampling switch connecting a data signal line to a video signal line such that the p sequential data signal lines of each data line group are connected to the same video signal line and p sequential data signal lines are alternately connected to the same video signal line with an interval of another ((n-1) x p) data signal lines therebetween, the p sampling switches associated with a given data line group each configured to be responsive to a different sampling pulse;

p shift registers provided with respect to each data fetching block, the shift registers being connected between blocks such that the blocks are driven sequentially;

a sampling pulse generating section provided with respect to each data fetching block configured to generate p sampling pulses responsive to one or more timing pulses generated by the p shift registers provided with respect to the block, the p sampling pulses configured to fetch the multiphased video signal from the video signal lines into all data signal lines in the block;

the data signal line driving circuit performing:

a first driving in which the p shift registers in each block are driven sequentially to provide p sequential timing pulses and each sampling pulse in the block being responsive to a corresponding timing pulse such that the sampling pulses in the block are activated sequentially, and

a second driving in which only one shift register in the block is driven to provide one timing pulse and all sampling pulses in the block are responsive to the one timing pulse such that all sampling pulses in the block are activated simultaneously.

14. The data signal line driving circuit as set forth in claim 11, wherein the data signal line driving circuit includes stopping means for stopping operation of the shift registers not required in driving the data signal lines when performing the second driving.

19. A display device, comprising:

a display panel which includes (i) a plurality of data signal lines, (ii) a plurality of scanning signal lines provided so as to cross the data signal lines, and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines, a video signal for displaying an image being fetched from the data signal lines into the pixels in synchronism with a scanning signal supplied from the scanning signal lines, said video signal being retained and multiphased into a multiphased video signal supplied to the data signal lines via n, n>1, video signal lines;

a data signal line driving circuit for outputting the multiphased video signal to the data signal lines in synchronism with a predetermined timing signal; and

a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal; wherein

the data signal line driving circuit is configured to drive said plurality of data signal lines respectively so as to fetch the multiphased video signal via said video signal lines into the data signal lines and includes:

m, m>1, data fetching blocks configured to receive the multiphased video signal supplied in parallel to the data fetching blocks by the video signal lines;

each data fetching block configured to fetch the multiphased video signal into n data line groups and each data line group including p, p>1, sequential data signal lines and driving p corresponding sequentially adjoining sections of a display;

a plurality of sampling switches, each sampling switch connecting a data signal line to a video signal line such that the p sequential data signal lines of each data line group are connected to the same video signal line and p sequential data signal lines are alternately connected to the same video signal line with an interval of another ((n-1) x p) data signal lines therebetween, the p sampling switches associated with a given data line group each configured to be responsive to a different sampling pulse;

p shift registers provided with respect to each data fetching block, the shift registers being connected between blocks such that the blocks are driven sequentially;

a sampling pulse generating section provided with respect to each data fetching block configured to generate p sampling pulses responsive to one or more timing pulses generated by the p shift registers provided with respect to the block, the p sampling pulses configured to fetch the multiphased video signal from the video signal lines into all data signal lines in the block;

the data signal line driving circuit performing:

a first driving in which the p shift registers in each block are driven sequentially to provide p sequential timing pulses and each sampling pulse in the block being responsive to a corresponding timing pulse such that the sampling pulses in the block are activated sequentially, and

a second driving in which only one shift register in the block is driven to provide one timing pulse and all sampling pulses in the block are responsive to the one timing pulse such that all sampling pulses in the block are activated simultaneously.

21. A display device, comprising:

a display panel which includes (i) a plurality of data signal lines, (ii) a plurality of scanning signal lines provided so as to cross the data signal lines, and (iii) pixels provided on intersections of the data signal lines and the scanning signal lines, a video signal having a plurality of color signals for displaying an image being fetched from the data signal lines into the pixels in synchronism with a scanning signal supplied from the scanning signal lines, said video signal being retained and multiphased into a multiphased video signal supplied to the data signal lines via n, n>1, video signal lines; wherein

each video signal line includes a plurality of divisional video signal lines divided so as to respectively correspond to the color signals and each data signal line includes a corresponding plurality of divisional data signal lines;

a data signal line driving circuit for outputting the multiphased video signal to the data signal lines in synchronism with a predetermined timing signal; and

a scanning signal line driving circuit for outputting the scanning signal to the scanning signal lines in synchronism with a predetermined timing signal; wherein

the data signal line driving circuit is configured to drive said plurality of data signal lines respectively so as to fetch the multiphased video signal via said video signal lines into the data signal lines and includes:

m, m>1, data fetching blocks configured to receive the multiphased video signal supplied in parallel to the data fetching blocks by the video signal lines;

each data fetching block configured to fetch the multiphased video signal into n data line groups and each data line group including p, p>1, sequential data signal lines and driving p corresponding sequentially adjoining sections of a display;

a plurality of sampling switches, each sampling switch connecting a data signal line to a video signal line such that the p sequential data signal lines of each data line group are connected to the same video signal line and p sequential data signal lines are alternately connected to the same video signal line with an interval of another ((n-1) x p) data signal lines therebetween, the p sampling switches associated with a given data line group each configured to be responsive to a different sampling pulse;

p shift registers provided with respect to each data fetching block, the shift registers being connected between blocks such that the blocks are driven sequentially;

a sampling pulse generating section provided with respect to each data fetching block configured to generate p sampling pulses responsive to one or more timing pulses generated by the p shift registers provided with respect to the block, the p sampling

pulses configured to fetch the multiphased video signal from the video signal lines into all data signal lines in the block;

the data signal line driving circuit performing:

a first driving in which the p shift registers in each block are driven sequentially to provide p sequential timing pulses and each sampling pulse in the block being responsive to a corresponding timing pulse such that the sampling pulses in the block are activated sequentially, and

a second driving in which only one shift register in the block is driven to provide one timing pulse and all sampling pulses in the block are responsive to the one timing pulse such that all sampling pulses in the block are activated simultaneously.

In the abstract:

In the 6th line replace "shift resister" with "shift register".

In the specification:

Add the following paragraph at the end of the section headed "BRIEF DESCRIPTION OF THE DRAWINGS", that is after page 17, line 12.

> "Fig. 26 shows a table, "TABLE 1", comparing reduction of power consumption in low resolution versus high resolution driving modes between embodiments of the invention with (Fig. 1) and without (Fig. 13) shift register bypassing and a prior art circuit (Fig. 22)."

In the drawings:

Add Fig. 26. - A new drawing sheet, identified as Fig. 26, is attached. Note that this is the sheet submitted as "TABLE 1" when the application was filed, which has been revised to add the label "FIG. 26".

2. The following is an examiner's statement of reasons for allowance:

While it is the totality of the claim limitations that distinguish the invention from the prior art, examiner offers a comment on "the rejection not made": As described in previous office actions, JP2000-181394 to Sunao teaches, among other things, the same multiphased high and low resolution driving modes as does the instant application. However, it does so using the equivalent of one of the data fetching blocks of the instant application. While the creation of the high and low resolution sampling pulses within a block using shift registers according to a known method was shown to be obvious, examiner determined that, although the individual elements were all available in the prior art, the generation of a combination using multiple data fetching blocks to which video signal lines supply a multiphased video signal in parallel with shift registers being connected between blocks such that the blocks are driven sequentially required excessive hindsight.

Regarding the introduction of terminology in the claims not found in the specification:

Examiner found that, although the totality of the disclosure of the application including the figures is an adequate disclosure of the invention, the language of the specification is inadequate to produce claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention. Examiner required the introduction of new language and here seeks to mitigate the effect of this by providing reasoning and citations for some introduced terms and language.

Positive integer variables m, n and p are introduced to allow convenient reference to the numbers without repetition of the defining phrases.

n is used to represent the number of video signal lines carrying the multiphased video signal. The figures show n=2 with the video signal lines shown as DAT1 and DAT2 in the figures not explicitly making reference to color signals and as RD1-GD1-BD1 and RD2-GD2-BD2 in the figures making explicit reference to color signals. The use of the number of video signal lines to drive the number of groups in a block is drawn from the specification. For example, [0095] of the pre-grant publication teaches, "That is, two sequential data signal lines constitute each of the data signal line groups, connected to the video signal lines 11 and 12, and *the data signal line groups whose number is the same as the number of the video signal lines constitute a single block*. Here, (i) a data signal line group constituted of the data signal lines SL1 and SL2 and (ii) a data signal line group constituted of the data signal lines SL3 and SL4 make up a single block."

m is used to represent the number of data fetching blocks. Fig. 1 shows two data fetching blocks and a portion of a third data fetching block

and Fig. 19 extends Fig. 1 to show explicit connections for color signals and shows the connections for one data fetching block and a portion of a second data fetching block.

p is used to represent the number of sequential data signal lines in a signal line group. The terminology of the claims as originally filed was "*a predetermined number* of the data signal lines". In the figures this number is 2, i.e. with groups made up of SL1-SL2, SL3-SL4 in Fig. 1, or (RSL1-GSL1-BSL1)-(RSL2-GSL2-BSL2) in Fig. 20.

The phrase "and each data line group including p, p>1, sequential data signal lines *and driving p corresponding sequentially adjoining sections of a display*" is introduced. The driving of sequentially adjoining sections by corresponding sequential data signal lines can be seen for example in Fig. 21 which shows sequential data signal lines SL1-SLx driving sequentially adjoining sections of a display. In this case the sections are columns and the first and second columns are adjoining as are the second and third columns and so forth and thus the columns are "sequentially adjoining". Although applicant's disclosure consistently uses - "sequential" data signal lines - or - "sequentially connected" data signal lines – in a way that implies that these are data signal lines that drive sequentially adjoining sections of the display, i.e. sections that can be combined to form a single section during low resolution driving, examiner believes that the range of ordinary meanings for "sequential" modifying "data signal lines" is great enough to require that the "read in light of the specification" meaning be made explicit in the claims. (adjoining. adjective, sharing a common boundary, (2003). In Roget's II The New Thesaurus. Retrieved from http://www.credoreference.com/entry/hmrogets/adjoining by examiner on September 3, 2009)

The phrase "p sequential data signal lines are alternately connected to the same video signal line with an interval of another ((n-1) x p) data signal lines therebetween" is introduced. An example of this arrangement can be seen in Fig. 1 in which data signal lines are alternately connected to each video signal line in groups of two. Thus for a given video signal line, i.e. DAT1: n sequential data signal lines (SL1-SL2 then SL5-SL6 etc.) are alternately connected to the same video signal line with an interval of another ((n-1) x p) data signal lines therebetween, i.e. two data signal lines SL3-SL4 are connected therebetween SL1-SL2 and SL5-SL6). The "((n-1) x p)" method of describing the number of sequential data lines between each group of sequential data lines connected to a given video signal line allows for the claim language to cover extension of the invention to more than two video signal lines as well as groups of more than two sequential data signal lines. The specification as filed covers this, for example, at the specification describes at [0208] of the pre-grant publication a case in which n=3 or more and at [0209] of the pre-grant publication a case in which p=3 or more:

> [0208] Note that, each of the aforementioned embodiments describes the case where the two-phase development is performed with respect to a video signal, but it is possible to obtain the same effect by performing development of three or more phases.
>
> [0209] Further, the number of the data signal lines connected to the video signal line, i.e., the number of the data signal lines in the data signal line group is two, but it may be so arranged that the number is three or more. For example, if the number of the data signal lines connected to the video signal line is three, it is possible to reduce the maximum resolution (high resolution) of the display section to 1/3.

The fact that the examiner, who is arguably below the level of ordinary skill in the art, was able to deduce, given applicants disclosure, the structure of the invention when applied with the number of video signal lines, the number of sequential data signal lines in each group, or both, being greater than 2, seems sufficient evidence that the new language does not introduce new matter.

The phrase "each video signal line including a plurality of divisional video signal lines divided so as to respectively correspond to the color signals *and each data signal line including a corresponding plurality of divisional data signal lines*" is introduced to explicitly include color signals in claims 2, 11 and 21. In particular, the term "divisional data signal lines" was not used in the specification but the correspondence between "video signal line" DAT1 in Fig. 1 and "divisional video signal lines" RD1-GD1-BD1 in Fig. 20 seems to apply equally well to "data signal line" SL1 in Fig. 1 and "divisional data signal lines" RSL1-GSL1-BSL1 in Fig. 20. With both the inputs and outputs of "an associated sampling switch" being defined, it seems unnecessary to point out in the claims that each sampling switch includes a plurality of divisional sampling switches.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Allowable Subject Matter

3. Claims 1-3, 6, 11, 14, and 19-22, now renumbered 1-10, allowed.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US 2002/0057251 to Higashi teaches multiple lines attached to the same video signal line so that adjacent pixel columns are not driven at the same time but doesn't teach a change of resolution.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROBERT R. RAINEY whose telephone number is (571)270-3313. The examiner can normally be reached on Monday through Friday 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on (571) 272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/RR/

/Amare Mengistu/

Supervisory Patent Examiner, Art Unit 2629